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A NOVEL METHOD FOR IMPROVING HOT CARRIER LIFETIME VIA A NITROGEN IMPLANTATION PROCEDURE PERFORMED BEFORE OR AFTER A TEOS LINER DEPOSITION

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to methods used to fabricate semiconductor devices, and more specifically to an ion implantation procedure, used to improve the reliability of metal oxide semiconductor field effect transistor, (MOSFET), devices, in regards to a hot electron carrier phenomena.

(2) Description of Prior Art

Micro-miniaturization has allowed the semiconductor industry to fabricate MOSFET devices with sub-quarter micron features. Specific MOSFET devices, such as input/output, N channel, (I/O NMOS), devices, used for logic applications, can however be prone to a hot electron carrier, (HCE), reliability phenomena. The I/O NMOS devices, operating at a voltage of 3.3, or 2.5 volts, can suffer gate insulator degradation, as a result of hot electron injection at these operating voltages. The substrate current, or drain current specifications are therefore difficult to satisfy, as a result of the HCE phenomena, for sub-quarter micron, I/O NMOS devices, operating

at 3.3, or 2.5 volts. Methods of annealing the gate insulator layer, in an NO or N_2O ambient, have not resulted in reductions in substrate current, (Isub), while other methods such as only providing a more graded, lightly doped source/drain, (LDD), region, have also not delivered the improved reliability of I/O NMOS devices, regarding HCE injection.

This invention will describe a novel process used to alleviate HCE injection, entailing the implantation of nitrogen, (N_2), or nitrogen ions, (N^+), either prior to, or after deposition of a silicon oxide layer, obtained using tetraethylorthosilicate, (TEOS), as a source, with the TEOS layer used as a liner layer, prior to formation of composite insulator spacers. The nitrogen implantation, located adjacent to the gate structure, and at the interface of a silicon oxide layer, underlying the composite insulator spacer, and an underlying lightly doped source/drain region, reduces HCE injection, as a result of nitrogen pile-up, at this interface. In addition the implantation procedure allows an increase in transient enhanced diffusion, (TED), to occur, resulting in a greater degree of LDD grading, than offered by counterparts fabricated without this nitrogen implant, thus reducing Isub, indicating a reduction of HCE injection. Prior art, such as Gardner et al, in U.S. Pat. No. 5,994,175, as well as Arai et al, in U.S. Pat. No. 5,972,783, describe nitrogen implantation prior to LDD formation, not however describing this present invention of implanting nitrogen, post LDD implantation, performed either prior to, or after deposition of a TEOS liner, used underlying a subsequent composite insulator layer.

SUMMARY OF THE INVENTION

It is an object of this invention to improve the reliability of sub-quarter micron, I/O NMOS devices, operating at 3.3 and at 2.5 volts, via reducing HCE injection.

It is another object of this invention to implant nitrogen, or nitrogen ions, near the top surface of the LDD region, prior to, or after, deposition of a TEOS oxide layer, to be used a TEOS liner, underlying a subsequently formed composite insulator sidewall spacer.

It is still another object of this invention to ion implant the LDD dopants, than in situ implant nitrogen, prior to, or after, deposition of the TEOS liner.

In accordance with the present invention, a method of implanting nitrogen, near the top surface of an LDD region, prior to, or after deposition of a TEOS liner, is described. A first iteration of this invention entails forming a polysilicon gate structure, on an underlying silicon dioxide gate insulator layer, and after an polysilicon re-oxidation step, a photoresist shape is used to block MOSFET core devices from an implantation procedure used to create an LDD region for I/O NMOS devices. After deposition of a silicon oxide layer, using TEOS as a source, another photoresist shape is again used to block core MOSFET devices, from a N_2 or a N^+ implantation procedure, placing the implanted species at a silicon oxide layer - LDD interface, for the I/O NMOS devices. Deposition of a silicon oxide layer, and of a silicon nitride layer, are followed by an anisotropic reactive ion etching, (RIE), procedure, resulting in a composite insulator spacer, overlying the TEOS liner, and on the sides of the I/O NMOS polysilicon gate structure, and

overlying the nitrogen implanted, LDD region.

A second iteration of this invention uses only one photoresist shape, to block the MOSFET core devices, from a series of in situ ion implantation procedures, comprising the implant procedure used to form the I/O NMOS, LDD region, followed by the in situ nitrogen implant. These implantations can be performed prior to, or after deposition of the TEOS liner.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiments with reference to the attached drawings that include:

Figs. 1 - 5, which schematically, in cross-sectional style, describe a first iteration of this invention, featuring the use of nitrogen, implanted into a top surface of a I/O NMOS, LDD region, after deposition of a TEOS liner layer.

Figs. 6 - 7, which schematically, in cross-sectional style, describe a second iteration of this invention, featuring the use of nitrogen, implanted into a top surface of a I/O NMOS, LDD region, prior to the deposition of a TEOS liner layer, however saving a photoresist masking step by in situ implanting the dopants for the LDD region, and nitrogen.

Fig. 8, which compares the profile of LDD regions formed with and without the nitrogen implantation procedure.

Fig. 9, which graphically describes the substrate current, of I/O NMOS devices, fabricated with, and without the nitrogen implantation procedure, described in this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of fabricating an I/O NMOS MOSFET device, with improved reliability, in terms of HCE injection, via a nitrogen implantation procedure, performed prior to, or after, the deposition of a TEOS silicon oxide layer, used between an underlying LDD region, and an overlying composite insulator spacer, will now be described in detail. A P type, semiconductor substrate 1, comprised of single crystalline silicon, with a <100> crystallographic orientation, is used and schematically shown in Fig. 1. A gate insulator layer 2, comprised of silicon dioxide, at a thickness between about 40 to 80 Angstroms, is thermally grown in an oxygen - steam ambient, at a temperature between about 650 to 900° C. A polysilicon layer is next deposited via low pressure chemical vapor deposition, (LPCVD), procedures, at a thickness between about 1500 to 2500 Angstroms. The polysilicon layer is either doped in situ, during deposition, via the addition of arsine, or phosphine, to a silane ambient, or the polysilicon layer is deposited intrinsically then doped via implantation of arsenic, or phosphorous ions. Conventional photolithographic and anisotropic, reactive ion etching, (RIE), procedures, using Cl_2 or SF_6 as an etchant are used to define polysilicon gate structure 3, schematically shown in Fig. 1. The photoresist shape used to define polysilicon gate structure 3, is removed via plasma oxygen ashing and careful wet cleans, with the wet clean cycle removing the exposed regions of gate insulator 2, not covered by polysilicon gate structure 3. An oxidation procedure is next performed to form

silicon oxide layer 4, on the surface of polysilicon gate structure 3, as well as on the exposed surface of semiconductor substrate 1. Silicon oxide layer 4, at a thickness between about 15 to 80 Angstroms, is obtained via thermal oxidation procedures, at a temperature between about 800 to 1015° C, in an oxygen-steam ambient.

A first iteration of this invention is next described, and shown schematically in Figs. 2 - 5. In addition to the fabrication of the I/O NMOS devices, the fabrication of core devices are also integrated on the same semiconductor chip. The core devices, not shown in the drawings, are designed with performance and reliability parameters, different than the performance and reliability requirements of the I/O NMOS devices. Therefore specific regions of the core devices, such as a previously formed lightly doped source/drain region, (LDD), have to be protected from subsequent I/O NMOS process steps, such as formation of the I/O NMOS LDD regions, and the critical nitrogen implantation procedure. Therefore prior to the formation of the I/O NMOS, LDD region 5, a photoresist block out shape, not shown in the drawings, is use to protect the core devices. LDD region 5, shown schematically in Fig. 2, is formed via ion implantation of arsenic or phosphorous ions, at an energy between about 20 to 50 KeV, at a dose between about 2E13 to 5E13 atoms/cm^2. This ion implantation procedure can be performed at an angle between about 0 to 45 degrees. After removal of the photoresist shape used to protect the core devices from implantation procedures used to form LDD region 5, via plasma oxygen ashing and careful wet cleans, TEOS liner 6, is deposited via LPCVD, or via plasma enhanced chemical vapor deposition, (PECVD), procedures, at a temperature between about 700 to 800° C, at a thickness between about 80 to 250 Angstroms, using tetraethylorthosilicate, (TEOS), as a source.

This is schematically shown in Fig. 2.

Another photoresist shape is used to protect the core devices from a critical implantation of nitrogen, (N_2^+), or nitrogen ions, (N^+), performed at an energy between about 5 to 25 KeV, at a dose between about 1E14 to 1E15 atoms/cm^2, resulting in a concentration of nitrogen ions 7, located at the top surface of LDD region 5. This is schematically shown in Fig. 3. This plantation procedure results in a pile-up of nitrogen at the LDD - oxide interface, reducing hot carrier electron, (HCE), injection, during operation of the completed I/O NMOS device. In addition the nitrogen pile-up, at this interface increase the transient enhanced diffusion, (TED), phenomena, allowing a more graded LDD region to be achieved, when compared to counterparts fabricated without the nitrogen implantation procedure. Graded LDD region 5, in combination with the nitrogen pile-up at the interface, also reduces HCE injection. The photoresist shape, used to protect the core devices from the nitrogen implantation procedure, is again removed via plasma oxygen ashing and careful wet cleans.

Composite insulator spacers are next formed, and schematically described using Figs. 4 - 5. Silicon nitride layer 8, is first obtained, via LPCVD or PECVD procedures, at a temperature between about 700 to 780° C, at a thickness between about 200 to 400 Angstroms. This is followed by the deposition of silicon oxide layer 9, again via LPCVD or PECVD procedures, at a temperature between about 700 to 800° C, to a thickness between about 850 to 1100 Angstroms, using TEOS as a source. Anisotropic RIE procedures, using CHF_3 as an etchant for silicon oxide layer 9, and using Cl_2 as an etchant for silicon nitride layer 8, are employed to form the composite

insulator spacers, shown schematically in Fig. 5. An overetch cycle, for the definition of the composite insulator spacers result in removal the exposed regions of TEOS liner 6, and of silicon oxide layer 4. Heavily doped source/drain region 20, is next formed in regions of the semiconductor substrate not covered by polysilicon gate structure 3, or by the composite spacers, on the sides of the polysilicon gate structure. Heavily dopes source/drain region 20, shown schematically in Fig. 5, is formed via implantation of arsenic, or phosphorous ions, at an energy between about 40 to 60 KeV, at a dose between about 3E15 to 6.5E15 atoms/cm^2. A rapid thermal anneal, (RTA), procedure, performed at a temperature between about 1000 to 1050° C, for a time between about 5 to 15 sec, in a nitrogen or argon ambient, is used to activate the dopants in heavily doped source/drain region 20, as well as grading the profile of LDD region 5.

A second iteration of this invention also features the desired nitrogen pile-up, at the LDD - oxide interface, reducing HCE injection, however this iteration features the implantation of the I/O NMOS LDD regions, followed by an in situ implantation of nitrogen, using only one photoresist mask, thus reducing cost. After definition of polysilicon gate structure 3, followed by the re-oxidation procedure, resulting in the formation of silicon oxide layer 4, a TEOS liner layer 10, is deposited, via PECVD or LPCVD procedures, at a thickness between about 80 to 250 Angstroms. This is schematically shown in Fig. 6. A photoresist shape is then formed to protect the core devices from an ion implantation procedure used to form LDD region 11a, and from an in situ ion implantation procedure, used to form nitrogen region 11b. This is schematically shown in Fig. 7. LDD region 11a, and nitrogen region 11b, are formed using identical ion implantation species and conditions used to form LDD region 5, and nitrogen

a

region 7, respectfully, in the first iteration. Composite insulator spacers, and a heavily doped source/drain region, not shown in the drawings, are again formed using materials, and conditions, identical to those used in the first iteration to form heavily doped source/drain region 20, and the composite insulator spacers, comprised of TEOS oxide - silicon nitride. The I/O NMOS device, described in the second iteration, fabricated using one less masking step, then experienced in the first iteration, again results in the desired HCE injection reduction, as a result of the nitrogen implantation procedure. If desired the implantation procedures used for creation of LDD region 11a, and for creation of nitrogen region 11b, can be accomplished prior to deposition of TEOS liner layer 10.

Fig. 8, graphically represents the dopant profile for LDD region 13, obtained using the nitrogen implantation procedure, featured in the two iterations of this invention. The more graded profile of LDD region 13, compared to counterpart LDD region 12, formed without the nitrogen implantation procedure, resulting from enhanced TED phenomena, will reduce HCE injection. This is shown in Fig. 9, where time to fail, (TTF), influenced by HCE injection, is shown against unwanted substrate current , (Isub), which is in turn generated by HCE injection. The TTF is increased for samples 15, formed using the nitrogen implantation procedure, when compared to samples 14, formed without the nitrogen implantation procedure, featured in this invention. Less substrate current, or less HCE injection is encountered as a result of the nitrogen pile-up, and graded LDD profile, accomplished via the procedures described in this invention.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit or scope of the invention.

What is claimed is: